What is claimed is:

1. A method of making a wafer scale package for electronic circuits, comprising the steps of:

placing electronic circuits each having at least one electronic device and associated signal lines at respective locations on a base wafer;

forming cavities on the undersurface of a cover wafer at respective locations to accommodate said respective electronic devices, when said wafers are joined;

forming and metalizing vias in said cover wafer;

metalizing the periphery of each said location on said base and cover wafers;

metalizing an electric contact between the bottom of a said metalized via and said signal lines;

joining said base and cover wafers at predetermined pressure, temperature and time conditions to form a peripheral hermetic seal around each said location and a via hermetic seal around each said bottom of a said via; and

dicing said joined and sealed wafers along said locations to provide individual die packages.

2. A method of making a wafer scale package according to claim 1 which includes the step of:

providing a base wafer of quartz.

3. A method of making a wafer scale package according to claim 1 which includes the step of:

providing a cover wafer of quartz.

4. A method of making a wafer scale package according to claim 1 which includes the step of:

metalizing the periphery of each said location on said base and cover wafers with a plurality of metal layers which include indium and nickel.

5. A method of making a wafer scale package according to claim 1 which includes the step of:

applying an initial metal layer of titanium on the top surface of said base wafer around the periphery of each said location; and

applying an initial metal layer of titanium on the undersurface of said cover wafer around the periphery of each said location.

6. A method of making a wafer scale package according to claim 1 which includes the step of:

joining said base and cover wafers at a pressure of around 30 to 80 psi.

7. A method of making a wafer scale package according to claim 1 which includes the step of:

joining said base and cover wafers at a temperature of around 120° C to 200° C.

8. A method of making a wafer scale package according to claim 1 which includes the step of:

joining said base and cover wafers at said predetermined pressure and temperature for around 1 to 3 hours.